In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 1, lines 14 to 18 as follows:

--The TI Wizard is a full Duplex SERDES (Serialize-Deserialize) function plus the high speed differential I/O, the built-in self test (BIST) circuitry, and the ~~PLL~~ phase locked loop (PLL) and ~~DLL~~ delay locked loop (DLL) circuitry needed for timing references for the SERDES. A Wizard port supports data rates from 1.0 Gbaud through 2.5 Gbaud. It also includes comma detect circuitry used for the byte alignment of incoming bit stream.--

A2

Rewrite the paragraph at page 1, lines 19 to 31 as follows:

--~~Functionality wise, the~~ The Wizard performs basically a Fibre Channel operation: Transmit is 10-bits of 8b/1 0b encoded data in and 1 bit at 10 x the frequency differential out. Receive is a 10x speed serial bit stream in and 10-bit 8b/1 0b data out. The receive side also performs byte alignment. Wizard is also intended to be used as the Physical Interface Portion of the 800 Mb 1394 standard, as well as Gigabit Ethernet, board to Board interconnect, DSP test port interface, ~~Chip~~ chip to chip interconnect, and any application that requires a very high speed serial interface. The primary intended application for Wizard is to provide building blocks in the ASIC library for developing point-to-point baseband data transmission over controlled impedance media of approximately 5052. The transmission media can be printed circuit boards, copper cables or fiber-optical media. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.--

A3

Rewrite the paragraph at page 2, lines 11 to 17 as follows:

--As shown in Figure 1, ~~PLL~~ a phase locked loop (PLL) is used for clock multiplication and ~~DLL~~ a delay locked loop (DLL) is used for clock recovery. The speed of the reference clock (REFCLK) of the PLL is 100-250 MHz depending upon the ASIC or board speed of the data link. Transmit path registers the parallel data TD<0:9> at the rising edge of REFCLK, does the parallel to serial conversion and sends the serial data through the transmitter at both edges of the TX clock. Receive path receives serial data and does serial to parallel conversion using the RX clock.--

A4

Rewrite the paragraph at page 4, lines 6 to 19 as follows:

--A time division multiplex data recovery system using a closed-loop phase ~~lock loop(PLL)~~ locked loop (PLL) and a delay locked ~~loop(DLL)~~ loop (DLL). In other words, one closed loop comprises both a phase locked loop (PLL) and a delay locked loop (DLL) in a novel time division multiplex data recovery system. This new architecture comprises a 4 stage Voltage Controlled Oscillator (VCO) used to generate 8 clock signals, 45 degrees phase shifted from one another, for 8 receivers ~~41~~ to do the oversampling in the data recovery block ~~40~~. The receivers ~~41~~ each trigger on only the rising edge of the clock to alleviate duty cycle issues. A phase interpolator 44 tracks the received data signal and feeds it back to the Phase/Frequency Detector (PFD) 34 to adjust the measurement position of the sampling clock 70. The PFD 34 has a second input of the reference clock which the PFD uses along with the interpolator input to correct the frequency and phase of the PLL. The PLL operates at a high bandwidth. The DLL's bandwidth is several orders lower than the PLL. The DLL activates only a multiplexer and an interpolator continuously, thereby drawing a minimum amount of power.--

A5

Rewrite the paragraph at page 5, lines 32 to 33 as follows:

A6 --Figure 12 illustrates a simplified phase select block diagram which illustrates the operation of the Phase ~~Select State Machine~~ interpolator 44 of Figure 3.--

Rewrite the paragraph at page 6, lines 5 to 6 as follows:

A7 --Figure 13 illustrates the 16-bit thermometer code 82 distributed equally between two input clock signals of the Phase ~~Select State Machine~~ interpolator 44 of Figure 3.

Rewrite the paragraph at page 6, lines 7 to 9 as follows:

A8 --Figure 14 illustrates the 8 octants of the phase diagram of the 8 states(clock signals) which are coded into the 3-bit octant code of the Phase ~~Select State Machine~~ interpolator 42 of Figure 3.--

Rewrite the paragraph at page 6, lines 10 to 11 as follows:

A9 --Figure 15 illustrates, in more detail, the block of circuitry in Figure 12 used to correct for invalid codes in the Phase ~~Select State Machine~~ interpolator 42 of Figure 3.--

Rewrite the paragraph at page 7, lines 15 to 20 as follows:

A10 --The Phase Locked Loop (PLL) 30 design consists of a phase/frequency detector 34, a differential charge pump, an on chip loop filter capacitor 36, a replica-feedback current source bias, a differential voltage controlled oscillator (VCO) 38, differential to single end buffer stages and a divide by five circuit block 46. The PLL 30 operates at 1.25 GHz, worst case, and minimizes the clock jitter caused by 250 MHz with 250 mV of low frequency square wave supply noise.--

Rewrite the paragraph at page 7, lines 26 to 31 as follows:

--where : y is the ratio of the small signal resistance of loop filter resistance of symmetric load in the delay element in the Voltage Controlled Oscillator (VCO), x is the ratio of charge pump current to the bias current set in the delay element of the VCO, N is the VCO frequency multiplier, ~~C1~~ C_1 is loop filter capacitance, ~~CB~~ C_B is the total effective capacitance of VCO ring oscillator and ~~C2~~ C_2 is the third order-roll off capacitance. The loop bandwidth to operating frequency ratio is given by--

Rewrite the paragraph at page 8, lines 7 to 8 as follows:

--In the transceiver PILL 30 design, y = 3, x = 0.5, N = 5, ~~C1~~ C_1 = 12 pf, ~~Cb~~ C_b = 0.372 pf, ~~C2~~ C_2 = 0.6 pf.--

Rewrite the paragraph at page 8, lines 9 to 28 as follows:

--As seen from left to right in Figure 3, the Phase Frequency Comparator (PFD) 34 will assert equal and short duration pulses at the outputs when both inputs are in phase. These pulses will help eliminate a dead-band in phase to frequency conversion which will lead to additional input tracking jitter. Since the outputs of PFD 34 (UP and DN) are single ended signals, these two signals are converted into differential UPs and DNs signals by the Phase Splitter Buffer or the INV32 blocks, which are included in the PFD ~~block~~ 34 of Figure 3.. INV32 blocks generate two differential UPs and two differential DNs to drive two differential charge pumps. The differential UPs and DNs signal from the output of the INV32 blocks should be matched as close as possible to help achieve zero static phase offset in the differential charge pump. The differential charge pump circuit, included in the loop filter block of Figure 3, is composed of three identical differential pair stages. The two differential input stages reduce noise coupling from full swing UPs and DNs signals to nearly DC signal at the

charge pump output. The output differential pair sums the "phase-to-current conversion" currents at the loop filter node. Each differential pair consists of symmetric loads, two NMOS source coupled pair and NMOS current source which is driven by the current replica circuit output Vcn. Since the PLL 30 is capable of operating over a wide range of frequency and the differential charge pump is scaled inversely proportional with the operating frequency, the differential charge pump current is set high (i.e. ~250μa) at 2.6 Gbps operating frequency so that it does not go below 10μa when the operating frequency is low.--

A12 cont.

Rewrite the paragraph at page 9, lines 11 to 24 as follows:

--The replica feedback bias circuit, located in the loop filter 36 ~~block~~ of Figure 3, is used to generate Vcp and Vcn from the loop filter voltage Vctrl for application to the VCO 38 and the phase interpolator 44. There are two replica-feedback bias circuit blocks. One is used in the core PLL ~~30 (to~~ 30 (to bias the VCO 38) and the other is used for biasing the phase interpolators 44 of the transmitters and receivers. This scheme helps to keep the closed loop bandwidth of both replica feedback bias circuits high so that they can track power and substrate noises that can effect the PLL 30 jitter performance. Each replica feedback bias circuit consists of an amplifier bias, a common source PMOS differential amplifier, a half buffer replica circuit and a loop filter control Vctrl voltage buffer. The transistors in loop filter 36 control Vctrl voltage buffers are adjusted so that 1/gm of the PMOS transistors is the desired feed-forward zero resistor value. Since the replica-feedback circuits are self-biasing circuits, bias start up circuit is essential to jump start the replica-feedback bias circuits which in turn initialize the PLL circuit properly.--

A13

Rewrite the paragraph at page 9, lines 25 to 31 as follows:

--The core of the VCO 38 consists of 4 differential delay elements 50, 52, 54 and 56 connected in a ring (Figure 4). The differential output at each node in the ring is buffered by three more stages of delay element at 1x, 2x, and 3x of the core delay element buffer strength. Each differential delay element consists of an NMOS source coupled pair, a current source NMOS bias by Vcn and a pair symmetric load. Each symmetric load consists of a diode-connected PMOS device in shunt with an equally sized Vcp biased PMOS device.--

A14

Rewrite the paragraph at page 10, line 31 to page 11, line 19 as follows:

--The ~~early/ate~~ early/late voting logic, illustrated in Figures 8 through Figure 11 or more comprehensively Figures 5 through Figure 11, is present in the data recovery block 40 of Figure 3. The purpose of the early/late voting logic is to determine whether the high speed sample clock of the receiver 41 is early or late relative to the 'ideal' temporal position of the sampling clock. The high speed clock that is used to sample the deserialized data stream will be referred to as the 'sampling clock" 70. The high speed clock that leads the sampling clock by 90 degrees will be referred to as the 'leading clock' 72. The ideal placement of the sampling point would be such that the high speed data is sampled right in the middle of the data bit's eye opening as illustrated in Figure 5a where the sampling clock 70 is located. The early/late voting logic uses a high speed clock that leads the high speed sampling clock by 90 degrees, so that the high speed data sampled by this leading clock 72 would be sampled deliberately right in the middle of the data crossings in the eye diagram as illustrated in Figure 5. This data, sampled by the leading clock 72, is compared to the data sampled by the sampling clock 70 to determine whether

A15

A15 Cont.

the sampling clock is early or late. The output of the early/late voting logic controls the phase select logic circuitry 42. The phase interpolator 44, early/late voting logic and phase select logic circuitry 42 all comprise a ~~digital~~ delay locked loop 32.--

Rewrite the paragraph at page 11, line 31 to page 12, line 13 as follows:

--The early/late voting logic is constructed in a pipelined fashion, two bits at a time. The input clock is the half-speed half baud rate clock, with rising edge leading the sampling clock 70 by 90 degrees. The first function is to determine from the data bits I whether the sampling clock 70 is early or late in the bit period as illustrated in Figures 5 and 7. Then these early or late indications are summed in pipelined fashion. This sum is accumulated over an 8-bit window. The early sum over an 8 bit window is ~~compare~~ compared to the sum of the late indications. If there are more early indications, then the early/late voting logic indicates an early vote. If there are more late indications, then the early/late voting logic indicates a late vote. The logic also derives a byte clock ~~form~~ from the high speed clock by doing a divide by 4 (as earlier stated). The early/late voting result is output for every 8-bits of the data stream, and is provided synchronous to the early/late output byte clock.--

A16

Rewrite the paragraph at page 12, line 30 to page 13, line 7 as follows:

--Figure 8 illustrates the first stage of the early/late pipeline, where the data bit sampled with the sampling clock 70 is compared ~~tot he~~ to the data bit sampled with the leading clock 72. PHINO and PHIN1 are the data sampled by the leading 72 or voting clock 72, while RXBITINO and RXBITIN1 are the data sampled by the sampling clock 70. An XOR gate is all that is needed to do the

A17

A17 Cont.

compare. Because of the half-baud rate clocks, the pipeline compares two bits at a time.--

Rewrite the paragraph at page 15, line 20 to page 16, line 15 as follows:

--Noteworthy is that the leading phase clock 72 is deliberately sampling the incoming data right at the ideal transition point. This is not normally the desired operation. The incoming data is being deliberately sampled right at the ideal data transition point. This is deliberately violating stable set-up and hold conditions on the flip flops that the data is being clocked into, leading to potentially unstable conditions. In reality, the data transitions will jitter around the ideal edge placement in practice so many times the data will be sampled accurately with the leading phase clock. On many other occasions this will ~~no~~ not be so, however. ~~the~~ The rationale is that on those occasions that the leading edge does catch the data right on transition, it does not matter whether the data was caught correctly or not. In this case, the metastable sampling of the data indicates that the leading edge clock is precisely positioned where it should be anyway. Since the phase select logic 42 MUST take a phase step early or late, either one will be a step away from ideal, and it does not matter which is chosen. It is expected that on the next phase update, the phase select logic 42 will step back towards the ideal sampling point again. Thus, there is a measure of built-in jitter on the recovered clock. The only remaining concern is that the early/late voting logic and the phase select logic 42 be implemented in such a way as to not get into an invalid or damaging state in the presence of metastable logic conditions internally. Due to the pipelined nature of the early/late voting logic, metastable logic conditions will not throw the logic into an invalid state and the depth of the pipelined logic actually helps to provide settling time for any

A18

metastable logic condition to settle down before it can propagate through to the phase select logic. The remaining concern is that the Phase Select Logic Block 42 can be constructed such that it is tolerant of potentially metastable conditions on the early/late voting result. That topic will be covered in the documentation for the phase select logic 42.--

A18 Cont.

Rewrite the paragraph at page 17, lines 7 to 13 as follows:

--Figure 12 illustrates the operation of the state machine of Phase Select ~~state machine~~ block 42. A bank of 16 flip flops contain a 16-bit 'thermometer code' 82 that controls the interpolation section of the phase interpolators 44. An additional three flip flops hold a 3 bit code that selects the multiplexing of the 8 clock phases into the phase interpolators 44. The total 19-bit register is operated as a state machine, where each state in the state machine determines the next state, depending upon the value of the EARLYB voting result from the Early/Late Voting block.--

A19

Rewrite the paragraph at page 17, lines 22 to 32 as follows:

--On the clock cycle where the phase is updated, the only choices for the new phase is the 'up' phase or the 'down' phase, depending upon the state of the EARLYB input. The EARLYB input controls a multiplexer that selects the new state, with a high level selecting the down (earlier) state and a low level selecting the up (later) state. The 2-input multiplexers controlled by the EARLYB signal are placed closest to the state flip flops in order to minimize set-up/hold requirements on the EARLYB signal relative to the clock input. Fewer multiplexers would be needed if the multiplexers controlled by the decimation phase in Figure 12 was placed closer to the flip flops, and the ~~ERALYB~~ EARLYB signal then controlled one set of multiplexers that selected between up and

A20

A20 Cont.

down states, but the extra multipliers were deemed worthy for the purposes of keeping the EARLYB set-up/hold requirements down.--

Rewrite the paragraph at page 18, lines 10 to 29 as follows:

--The 16-bit thermometer code 82 is used to select one of 17 possible phases between two input clocks. If the thermometer code 82 is 0000000000000000 then the resultant phase is 100% of the input clock and 0% of the second input clock. If the thermometer code 82 is 1000000000000000 then the resultant phase is -94% of the first input clock and -6% of the second input clock. If the thermometer code 82 is 1111111111111111 then the resultant phase is 0% of the first input clock and 100% of the second input clock. See Figure 13 for illustration. At the code 1111111111111111, 0% of the first input clock is used to determine the resultant phase, and so at this code the mux input to the phase interpolator may by switched over to a third input clock with no change in the resultant phase. If the thermometer code 82 then becomes 1111111111111110, then the resultant phase is 94% of the second input clock and 6% of the third input clock. Thus the name thermometer code 82: the code rises from 0000000000000000 to 1111111111111111 as the phase interpolator is bumped 'up' in phase until the ~~muxs~~ muxes for the input phases are switched, and then the thermometer code 82 falls from 1111111111111111 down to 0000000000000000 as the phase continues to be bumped 'up'. thus in even numbered octants of the phase diagram (see Figure 14), a rising thermometer code 82 equates to moving 'up' in phase, while in odd numbered octants, a failing thermometer code 82 equates to moving 'down' in phase. This thermometer code is forwarded to the phase interpolator 44 for adjusting the phase of the sampling clock 70 accordingly.--

A21

Rewrite the paragraph at page 19, lines 17 to 23 as follows:

--There is block of circuitry in Figure 12 to correct for invalid codes. This circuitry is shown in more detail in Figure 15. Essentially, each bit of the code is ~~anded~~ ANDed with the bit preceding it in the code. If a one in the code is either a first bit of the code or follows a one bit in the code, then it is a valid code. If a one in the code is found to follow a zero, then that one is changed to a zero and then filtered out. In this way, if any invalid code, either from the initial power up states of the flip flops or due to circuit glitch or metastable EARLYB signal, is filtered out back to valid code.--

A22

Rewrite the paragraph at page 19, line 24 to page 20, line 6 as follows:

--The Phase Interpolator 44 illustrated in Figures 3, ~~16,17,and~~ 16, 17, and 19 receives two input clocks with a phase difference of 45 degrees from the VCO 38 and generates an output clock whose phase is the weighted sum of the phases of the two input clocks. It is designed to have 16 phase steps per 45 degrees (64 phase steps per bit ~~time)as~~ time) as illustrated in Figures 13 and 18. The thermometer code 82 that controls the digital weights is generated by the phase select logic 42. As shown in ~~figure~~ Figure 4, the four stage VCO 38 (delay elements are differential) produces 8 clocks which are 45 degrees apart. The phase interpolator 44 takes two adjacent phases and interpolates them to one of the 16 phases based on the digital weights. Two clock phases are selected by the phase select logic 42 and then interpolated by the interpolator based on the thermometer code ic(0:15) and ~~ic b(0:15)82,~~ ic b(0:15) 82, which are also generated by the phase select logic 42.--

A23

Rewrite the paragraph at page 20, lines 7 to 29 as follows:

--As shown in Figure 4, the four stage VCO 38(delay elements are differential) produces eight clock phases, ck0, ck1, ck2, ck3, ck4, ck5, ck6, ck7, which are each 45 degrees apart from one another. The interpolator takes two adjacent phases and interpolates them to one of the 16 phases based on the digital weight controlled by the thermometer code 82. As shown in Figure 16, two MUXes 80 select two adjacent vectors for interpolation. Top PHMUX 80 selects one vector out of four ~~(eP0, eP1, eM0 and eM1)~~ (ck0, ck2, ck4 and ck6) and bottom PHMUX 80 selects one vector out of the four remaining vectors ~~(oP0, oP1, oM0 and oM1)~~ (ck1, ck3, ck5, ck7). Since the signal path is differential, if ePO ck0 is selected (as the positive signal of the ~~differential)eM0~~ differential ck4 is the negative signal of the differential signal and ~~vica~~ vice versa. Both PHMUX 80 are identical and each comprise two more identical ~~mulitplexers~~ multiplexers within each PHMUX 80. The first multiplexer within selects either ~~eP0~~ ck0 or ~~eP1~~ ck2 and the later selects either ~~eM0 ck4~~ or ~~Em1~~ ck5 by simply inverting the output of the first MUX. Phase select logic 42 generates control signals sE0, sE1, ~~S00,~~ sO0 sO1, invE, invE_b, invO and invO_b, which determine which clock vectors are selected in such a way that only one vector is selected at one instance. For example, if the output clock phase is starting from 0 degrees and increasing (counter clockwise direction in Figure 18), ~~eP0~~ ck0 and ~~oP0~~ ck1 are the two vectors selected. When through thermometer inputs demanding an increasing phase shift the output clock reaches 45 degrees, ~~eP1~~ ck2 is selected instead of ~~eP0,~~ ck0 while ~~oP0~~ ck1 is still selected. Similarly, when the output clock reaches 90 degrees, ~~eP1~~ ck3 is selected instead of ~~oP0,~~ ck1 while ~~eP1~~ ck2 is still selected. The two selected clock phases, oep and oop in ~~figure~~ Figure 16 are interpolated by phase interpolator 44 based on the thermometer code

A24 Cont. ic(0:15) and ~~ic_b(0:15)82,~~ ic b(0:15) 82, which are generated by the phase select logic 42.--